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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/724,012	11/26/2003	Francois Icher	STMI07-02207	7559

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EXAMINER	
LEJA, RONALD W	
ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 08/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/724,012	ICHER ET AL.	
	Examiner	Art Unit	
	Ronald W. Leja	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/6/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claims 1-6 are objected to because of the following informalities: Starting in line 22 of Claim 1 and in line 23 of Claim 6, the text is considered to be mis-descriptive, since a part of each track is not partially located between a part of one diode only and the connection terminal. More correctly, one track is partially located between a first diode and the connection terminal and the other track is partially located between a second diode and the connection terminal. In Claims 1-6, reference to the surface of the substrate should probably be referenced to the "top" surface of the substrate, for clarity purposes, since a substrate is three-dimensional and can have connection terminals on the side surfaces. Appropriate correction is required.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Countryman et al. (5,514,892) in view of Pettersson (6,388,851).

Countryman et al. disclose a device for offering ESD protection to circuitry upon or connected to the substrate (32). Figure 1 illustrates the connection of diodes (i.e. 19 and 17) to the connection terminal (20). Figure 5 illustrates the use of multiple tracks (46, 48, 50, 52, 54 and 56) and the above diodes being located under the connection terminal (20). A first diode (17) has its cathode (30) linked to the (higher potential VDD) first track (56) and its anode (44) linked to the connection terminal (via the other diodes). A second diode (19) has its cathode (33) linked to the connection terminal, but not that its anode (32) is linked to the second track. However, in the instant Reference, the substrate (32) is grounded so as to avoid any RF interference, and therefore, does not rely upon a specific track for connection of the anode of the diode terminal. In spite-of-the-fact, Pettersson teaches (Fig. 1) the use of multiple tracks (33 and 35) wherein each is connected respectively to VDD and GND and are to allow for proper connection of protection diodes to the connection terminal (5). Therefore, it is the opinion of the Examiner that it would have been obvious to one having ordinary skill in the art at the time of the invention to incorporate the teachings of Pettersson and use a second track for facilitating the anode connection of the second diode for those applications not requiring the substrate to be grounded, and thereby offering ease in the connection of the IC to power supply (via tracks to side or upper surface terminals) and not to the bottom surface of the chip; this increases applications to those requiring less specific limiting IC connections, and thus, increasing sales. It also would have been obvious as a means to further increase the resistance to downward pressure when wire was being connected to the

connection terminal (20), thereby increasing de-lamination protection to the diodes, resulting in a more robust design. For Claims 1 and 6, the tracks (i.e. 46, 56) are located partially between the diodes and the connection terminal. For Claims 2 and 3, anode (44) of the first diode is surrounded by the cathode (30) and the cathode (33) of the second diode is surrounded by its anode (32). As far as passing various connections thru the tracks, such limitations would have been obvious as a means to meet the desired connections for the protection circuit being implemented in design by the particular IC. For Claim 8, the use of a voltage limiter for ESD protection is well known in the art. In fact, the diodes themselves are voltage limiters. It would have been obvious to incorporate any voltage limiter to any part of the ESD design so as to meet the desired protection level and protect from the anticipated discharges, thereby offering a reliable and durable IC design.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ronald W. Leja whose telephone number is (571)272-2053. The examiner can normally be reached on Monday thru Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571)272-2800. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Ronald W Leja
Primary Examiner
Art Unit 2836

8/6/06

rwl
August 6, 2006